REMARKS

Claims 21 to 58 were pending in the application at the time of examination. The title and the drawings stand objected to. Claims 21 to 31 stand rejected under 35 U.S.C. § 112, second paragraph. Claims 21 to 58 stand rejected as anticipated.

The title of the invention was objected to as not being clearly indicative of the invention to which the claims are directed. In view of the objection, Applicants have amended the title. Applicants respectfully request reconsideration and withdrawal of the objection to the title.

The drawings stand objected to under 37 CFR 1.83(a). The rejection stated in part:

> The drawings must show every feature of the invention specified in the claims. Therefore, speculatively locking a resource prior to hazard determination between portions of two instructions must be shown or the feature(s) canceled from the claim(s). Similarly, speculatively dispatching a load to a cache prior to RAW hazard determination and handling data from the cache based on the determination must be shown or canceled.

Applicants respectfully traverse the objection to the drawings. Applicants respectfully note that the requirement in the Rules in not as broad as implied in the rejection. In particular, Rule 1.83(a) states:

> **§ 1.81 Drawings required in patent application.**
> (a) The applicant for a patent is required to furnish a drawing of his or her invention **where necessary for the understanding of the subject matter sought to be patented**; (Bold and underlined emphasis added; Bold only emphasis in original.)

Thus, the rule requires a drawing only where necessary for the understanding of the subject matter sought to be patented. Applicants provided detailed drawings of the structure of the

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microprocessor as well as specific examples of entries in the load/store unit. Further, Applicants provided multiple pseudo code examples in the addendums.

Applicants respectfully submit that a drawing of an entry in a memory with a bit set to indicate a lock provides no meaningful information and the description describes how hazards are determined and in which stages of the pipeline. For example, "A load instruction can be speculatively dispatched to DCU 130 in the E stage even though the corresponding RAW hazards are not calculated until the C stage." Specification, pg. 15, line 14 to 16. This explicitly relates one embodiment of the invention to the drawings.

Accordingly, not only are additional drawings unnecessary for the understanding of the subject matter sought to be patented, but also the specification describes at least one example of the invention in relationship to the drawings. Accordingly, Applicants respectfully request reconsideration and withdrawal of the objection to the drawings.

Claims 21 to 31 stand rejected under 35 U.S.C. § 112, second paragraph. Applicants have amended Claim 29 as suggested by the Examiner. Applicants have also amended Claim 31 to provide a proper antecedent basis for the recited instruction. Applicants respectfully request reconsideration and withdrawal of the § 112 second paragraph rejection of Claims 21 to 31.

Claims 29 to 31 and 36 to 39 are amended to correct antecedent basis informalities.

Claims 21, 32, 42, 45, and 56 are amended to more clearly recite the invention.

Claims 22, 25 and 28 are amended to correct an antecedent basis informality introduced by the amendment of Claim 21.

Claims 34 and 40 are amended to correct an antecedent basis informality introduced by the amendment of Claim 32.

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Claim 46, 49, and 52 are amended to correct an antecedent basis informality introduced by the amendment of Claim 45.

Claims 21 to 56 and 58 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent Number 5,168,564, hereinafter referred to as Barlow. The rejection stated in part:

> 12, Referring to claims 21, 32, and 45 Barlow has taught a method comprising; speculatively locking a resource to be accessed by execution of a first instruction, wherein the locking is performed prior to determining whether a hazard exists between the accessing portion of the first instruction and a portion of a second instruction based, at least in part, on order of the first instruction with respect to the second instruction. See Barlow, column 1, lines 50-61, and column 2, lines 40-64; note that the locking is speculative because the system speculates that a hazard will exist among first and second RMW operations in the future, and therefore, it must lock the resource speculatively (ahead of time) in order to fix any hazard associated with the second instruction's access/execution following the first instruction's access of data. It may turnout, however, that the locking has nothing to do with a hazard, but instead, with fixing a malfunctioning lock mechanism, which is done by locking a resource and then canceling read/write processing associated with that resource. See column 2, line 65, to column 3; line 5.

Applicants respectfully traverse the anticipation rejection of each of Claims 21, 32 and 45. In Col. 1, lines 50 to 61, Barlow taught:

> One way to prevent more than one processing unit from performing a RMW operation on the same memory location, an interlock read instruction is utilized. This involves the use of a lock indicator device, which is set during the read portion of an RMW operation to prevent access to a specific memory location, and is reset after the write portion of the RMW operation is completed. If a second processing unit should attempt to access the same memory location to perform an RMW operation, the memory subsystem will send a busy signal indicating that the memory location is in use.

Thus, Barlow taught that an actual access of the memory location was required to determine whether a hazard exists. This not only fails to teach the invention in the same level of detail as recited in these claims, but also teaches away from, for example:

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> determining, after said locking, whether a hazard exists between an accessing portion of the first instruction, when executed in said instruction pipeline, and a portion of a second instruction **based, at least in part, on order of the first instruction with respect to the second instruction as indicated in a entry for said first instruction in a buffer of a load/store unit of a processor including said instruction pipeline.**

The determining process in these claims makes accessing the memory location to determine whether there is a hazard unnecessary and so distinguishes over Barlow. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of each of Claims 21, 32 and 45 in view of Barlow.

Claims 22 to 31 depend from Claim 21 and so distinguish over Barlow for at least the same reasons as Claim 21. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of each of Claims 22 to 31 in view of Barlow.

Claims 33 to 41 depend from Claim 32 and so distinguish over Barlow for at least the same reasons as Claim 32. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of each of Claims 33 to 41 in view of Barlow.

Claims 46 to 55 depend from Claim 45and so distinguish over Barlow for at least the same reasons as Claim 45. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of each of Claims 46 to 55 in view of Barlow.

With respect to the anticipation rejection of Claim 42 in view of Barlow, the rejection stated:

> 24. Referring to claim 42 Barlow has taught a processor adapted to: a) speculatively dispatch a load operation to a cache unit prior to determining whether read-after-write hazards associated with the load operation are present (Barlow column 1 lines 50-61, column 2 lines 40-64; the lock indicator, or mechanism, can be canceled after being set once it is determined that the command using the resource that is

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> locked is invalid, therefore the resource is being locked before the command has been determined to have hazards, and before the command is known to go until completion, which goes along with the definition of prior to a determination of a hazard in the instant application at page 2 line 23-page 3 line 4 - the first portion of a read modify write is a read from memory, which is a load instruction).
> b) handle a datum from the cache unit for the speculatively dispatched load operation based, at least in part, on the determining. For a subsequent instruction seeking to access the same data as the load instruction, the data can be handled in one of two ways. If a hazard exists, then that data is not made available to the second instruction until the first read-modify-write (RMW) instruction (which includes the load) is finished with it. If there is no hazard (i.e., the second instruction does not need to use the data while the first RMW is operating on it), then the data will be made available to the second instruction.

Barlow, Col. 1, lines 50 to 61 were quoted above and that quotation is incorporated herein by reference. As noted above, in this section, Barlow taught that an actual access of the memory location was required to determine whether a hazard exists. This not only fails to teach the invention in the same level of detail as recited in Claim 42, but also teaches away from:

> determine, following said speculative dispatch, whether read-after-write hazards associated with the load operation are present based on information in an entry in a load buffer for said load operation;

This determining process makes accessing the memory location to determine whether there is a hazard unnecessary and so distinguishes over Barlow. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of Claims 42 in view of Barlow.

Claims 43 and 44 depend from Claim 42 and so distinguish over Barlow for at least the same reasons as Claim 42. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of each of Claims 43 and 44 in view of Barlow.

With respect to the anticipation rejection of Claim 56 in view of Barlow, the rejection stated:

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> 27. Referring to claim 56, Barlow has taught a method of speculatively locking a resource, the method comprising:
> a) dispatching for execution a load operation prior to determining whether a hazard exists between the load operation and a store operation indicated in a buffer. See column 1 lines 50-61, column 2 lines 40-64; the lock indicator, or mechanism, can be canceled after being set once it is determined that the command using the resource that is locked is invalid, therefore the resource is being locked before the command has been determined to have hazards, and before the command is known to go until completion, which goes along with the definition of prior to a determination of a hazard in the instant application at page 2 line 23-page 3 line 4. In order to detect a hazard between two instructions, a first instruction must be dispatched and executed. The first RMW instruction includes a load, (i.e., read). The second instruction includes a store (i.e., a write). So, in order to determine if the second RMW conflicts with the first, the first must be dispatched. Also, instructions are inherently stored in some buffer before dispatch.
> b) locking a resource of the load operation incident with execution of the load operation. See column 1, lines 50-61, and column 2, lines 40-64.
> c) determining whether the hazard exists and handling a datum returned for the load operation based, at least in part, on the determining. For a subsequent instruction seeking to access the same data as the load instruction, the data can be handled in one of two ways. If a hazard exists, then that data is not made available to the second instruction until the first read-modify-write (RMW) instruction (which includes the load) is finished with it. If there is no hazard (i.e., the second instruction does not need to use the data while the first RMW is operating on it), then the data will be made available to the second RMW.

Barlow, Col. 1, lines 50 to 61 was quoted above and that quotation is incorporated herein by reference. As noted above, in this section, Barlow taught that an actual access of the memory location was required to determine whether a hazard exists. This not only fails to teach the invention in the same level of detail as recited in Claim 46, but also teaches away from:

> determining whether the hazard exists based on information in an entry in a load buffer for said load operation

This determining process makes accessing the memory location to determine whether there is a hazard unnecessary and so distinguishes over Barlow. Applicants respectfully request

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reconsideration and withdrawal of the anticipation rejection of Claims 56 in view of Barlow.

Claim 58 depends from Claim 56 and so distinguishes over Barlow for at least the same reasons as Claim 56. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of Claim 58 in view of Barlow.

Claims 42 and 56 to58 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,420,991, hereinafter referred to as Konigsfeld. The rejection of Claim 42 stated in part:

> 30. Referring to claim 42, Konigsfield (Sic) has taught a processor adapted to:
> a) speculatively dispatch a load operation to a cache unit prior to determining whether read-after-write hazards associated with the load operation are present. See the abstract. Note that a load, which occurs after a store, when speculatively executed past the store, causes a RAW hazard which is ultimately detected.
> b) handle a datum from the cache unit for the speculatively dispatched load operation based, at least in part, on the determining. See the abstract and column 8, lines 4-16, and note that when a conflicting store is encountered (hazard occurs), the load has improperly executed, and consequently, the load is canceled (and the data it loaded is discarded). If a hazard does not exist, then the data was properly loaded and may be used by a subsequent instruction.

Applicants respectfully traverse the anticipation rejection of Claim 42 in view of Konigsfeld. The Abstract of Konigsfeld stated:

> An apparatus for maintaining processor ordering in a multi-processor computer system wherein loads are performed speculatively. Speculative loads of each processor are temporarily stored in their respective processors' load buffer. When one of the processors performs a store, a snoop operation is performed on the other processors' load buffers. If the snoop results in a hit, a determination is made as to whether that load buffer contains any prior conflicting speculative loads which have been completed. If the load buffer does contain a prior conflicting load, a processor ordering violation signal is generated. In response to this signal, the violating load and all subsequent operations are canceled and re-executed at a later time. (Emphasis Added)

This portion of Konigsfeld taught that a snoop process was required to examine each of the other processors' load buffers

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to determine a conflict. A snoop process on load buffers of other processors not only fails to teach the invention in the same level of detail as recited in Claim 42, but also teaches away from:

> determine, following said speculative dispatch, whether read-after-write hazards associated with the load operation are present based on information in an entry in a load buffer for said load operation;

This determining process makes the snoop process unnecessary and instead of looking in the load buffers of other processors uses information in the load buffer for the instant load operation and so distinguishes over Konigsfeld. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of Claims 42 in view of Konigsfeld.

With respect to the anticipation rejection of Claim 56 in view of Konigsfeld, the rejection stated:

> 31. Referring to claim 56, Konigsfield has taught a method of speculatively locking a resource, the method comprising:
> a) dispatching for execution a load operation prior to determining whether a hazard exists between the load operation and a store operation indicated in a buffer. See the abstract.
> b) locking a resource of the load operation incident with execution of the load operation. See column 6, line 66, to column 7, line 24, and column 8, lines 4-16. And note that a resource is locked, where the resource is related to execution of a load.
> c) determining whether the hazard exists and handling a datum returned for the load operation based, at least in part, on the determining. See the abstract and column 8, lines 4-1 *6*, and note that when a conflicting store is encountered (hazard occurs), the load has improperly executed, and consequently, the load is canceled (and the data it loaded is discarded). If a hazard does not exist, then the data was properly loaded and may be used by a subsequent instruction.

The Abstract of Konigsfeld was quoted above. As noted above, the Abstract of Konigsfeld taught that a snoop process was required to examine each of the other processors' load buffers to determine a conflict. A snoop process on load buffers of other processors not only fails to teach the

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invention in the same level of detail as recited in Claim 56, but also teaches away from:

> determining whether the hazard exists based on information in an entry in a load buffer for said load operation

This determining process makes a snoop process unnecessary and instead of looking in the load buffers of other processors uses information in the load buffer for the instant load operation and so distinguishes over Konigsfeld. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of Claims 56 in view of Konigsfeld.

Claims 57 and 58 depend from Claim 56 and so distinguish over Konigsfeld for at least the same reasons as Claim 56. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of each of Claims 57 and 58 in view of Konigsfeld.

Claims 21 to 58 remain in the application. Claims 21, 22, 25, 28 to 32, 34, 36 to 42, 45, 46, 49, 52, and 56 have been amended. Claims 1 to 20 were canceled previously. For the foregoing reasons, Applicant(s) respectfully request allowance of all pending claims. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicant(s).

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 19, 2007.

Attorney for Applicant(s) — October 19, 2007 Date of Signature

Respectfully submitted,

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